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10/679,752	10/06/2003	Jeffrey H. Burns	DP-310264	2820

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EXAMINER	
CUTLER, ALBERT H	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/679,752	BURNS, JEFFREY H.	
	Examiner	Art Unit	
	Albert H. Cutler	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is responsive to communication filed on May 29, 2007. Claims 1-19 are pending in the application.

Response to Arguments

2. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 11 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Amended claim 11 recites, "a thin film optical material **electrically** coupled to said substrate". However, paragraph 0026 of the specification recites, "thin film optical material 104 may be applied to a surface of substrate 102". This is also shown in figure 2, wherein the thin film optical material(104) is included between the lens housing(18) and optically transmissive substrate(102), neither of which are electrical components.

Therefore, according to the original disclosure, the thin film optical material is clearly not "electrically" coupled to the optically transmissive substrate. The Examiner will interpret claim 11 to read, "a thin film optical material coupled to said substrate".

Claim Rejections - 35 USC § 102

5. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

6. Claims 11-13, 15, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Melman et al.(US 6,564,018).

Consider claim 11, Melman et al. teach:

An optical sensor circuit assembly(figures 1-9b), comprising: an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49);

a thin film optical material coupled to said substrate(cover glass(106) has an antireflective coating(816, i.e. thin film), see figure 8b, column 6, line 57 through line 65);

an integrated circuit("semiconductor die" 116, column 5, line 46) having a face including an optical imaging element("sensor", 116, column 6, line 52, figure 8b), said face coupled with said substrate(The top face of optical imaging element(116) is coupled to substrate(806) with glue layer(800), see figure 8b).

Consider claim 12, and as applied to claim 11 above, Melman et al. further teach that said thin film optical material(816) comprises an antireflective material(column 6, lines 57-65).

Consider claim 13, and as applied to claim 11 above, Melman et al. further teach:

said thin film optical material(816) comprises an antireflective material(column 6, lines 57-65); and

said optically transmissive substrate(806) comprising a filter material dispersed in said substrate("Instead of using the IR coating an IR absorbing glass may be used(i.e. a substrate with IR material dispersed within)", column 7, lines 13-14).

Consider claim 15, and as applied to claim 11 above, Melman et al. further teache:

at least one lens("lens", 202, figure 3) positioned to direct electromagnetic radiation through said substrate and filter material and to said optical imaging element(see figure 3, column 4, lines 36-54).

Consider claim 16, and as applied to claim 15 above, Melman et al. further teach:

a lens mount("body", 300, see figure 3, the lens is coupled to the substrate via the body(300)) supporting said at least one optical("lens", 202, figure 3) and coupled to a second surface(top surface, see figure 3)) of said substrate(Said substrate is labeled

"106" in figure 3. Lens mount(300) is coupled to substrate(106) via film leads(302 and 304), column 4, lines 55-58.)

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 1-7, 9, 10, 17 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsin(US 2004/0150740) in view of Melman et al.(US 6,564,018).

Consider claim 1, Hsin teaches:

An optical sensor circuit assembly(figures 2 and 3, paragraphs 0011-0018), comprising:

an optically transmissive substrate("transparent layer", 60); and

an optical imaging element("photosensitive chip", 58) electrically coupled to said substrate(The optical imaging element(58) is electrically coupled to said substrate(60) via wires(68) and signal input terminals(64). See figures 2 and 3, paragraph 0013.).

Hsin further teaches of filter material("infrared filter", 86), but does not explicitly teach that said filter material is included in the optically transmissive substrate.

Melman et al. is similar to Hsin in that Melman et al. teach an optical sensor circuit assembly(figures 1-9b), comprising an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49), and an optical imaging element("sensor", 116, column 6, line 52, figure 8c) coupled to said substrate(sensor(116) is coupled to filter material(820) with glue layer(800), see figure 8c).

However, in addition to the teachings of Hsin, Melman et al. teach that the optically transmissive substrate includes filter material(cover glass(106) has an antireflective coating(816) and an optical IR blocking coating(820), see figure 8C, column 6, line 57 through column 7, line 6).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to include filter material as taught by Melman et al. in the optically transmissive substrate taught by Hsin for the benefit of preventing excess ghosting and scattered light as is caused by internal reflections of optically transmissive substrates, reducing the number of pieces of the optical sensor circuit assembly, preventing damage to the filter material due to the cleaning of the separate lens module, and correcting color and/or contrast distortion(Melman et al., column 2, lines 1-24, column 6, line 44 through column 7, line 2).

Consider claim 2, and as applied to claim 1 above, Hsin does not explicitly teach of filter material included in said optically transmissive substrate. However, Melman et al. further teach that said filter material is embedded in said substrate("deposited on internal surface(818, i.e. embedded) of glass cover(806, i.e. said substrate)", column 7, lines 3-5).

Consider claim 3, and as applied to claim 1 above, Hsin does not explicitly teach of filter material included in said optically transmissive substrate. However, Melman et al. further teach that said filter material is dispersed in said substrate("Instead of using the IR coating an IR absorbing glass may be used(i.e. the IR material is dispersed in the substrate)", column 7, lines 13-14).

Consider claim 4, and as applied to claim 1 above, Hsin does not explicitly teach of filter material included in said optically transmissive substrate. However, Melman et al. further teach that said filter material comprises a thin film layer on said substrate(The Anti-reflective portion on the filter material(816) is applied as a coat(i.e. a thin film layer) on the surface of the substrate(806), column 6, lines 57-65).

Consider claim 5, and as applied to claim 4 above, Hsin does not explicitly teach of filter material included in said optically transmissive substrate. However, Melman et

al. further teach that said thin film layer(816) further comprises material having antireflective properties(column 6, lines 57-65).

Consider claim 6, and as applied to claim 1 above, Hsin further teaches:

a circuit member(56) coupled to a first surface(bottom surface) of said substrate(60, see figures 2 and 3), said circuit member(56) defining a plurality of electrically conductive leads(64, 66, 68, paragraph 0013).

Consider claim 7, and as applied to claim 6 above, Hsin further teaches:

said optical imaging element(58) includes an integrated circuit(The optical imaging element(58) is a photosensitive chip(i.e. an integrated circuit).) and a plurality of electrically conductive pads(See figures 2 and 3, the optical imaging element(58) includes at least one electrically conductive pad on each side of the top surface thereof.), said plurality of pads coupled with corresponding ones of said plurality of leads(68, figures 2 and 3).

Consider claim 9, and as applied to claim 1 above, Hsin further teaches:

at least one optical element("lens", 84, figures 2 and 3) positioned to direct electromagnetic radiation through said substrate and filter material and to said optical imaging element(see figures 2 and 3, paragraph 0015).

Consider claim 10, and as applied to claim 9 above, Hsin further teaches a lens mount(46) supporting said at least one optical element(84, see figures 2 and 3). However, Hsin does not explicitly teach that the lens mount is coupled to a second surface of said substrate.

Melman et al. further teach a lens mount("body", 300, see figure 3, the lens is coupled to the substrate via the body(300)) supporting said at least one optical element("lens", 202, figure 3) and coupled to a second surface(top surface, see figure 3)) of said substrate(Said substrate is labeled "106" in figure 3. Lens mount(300) is coupled to substrate(106) via film leads(302 and 304), column 4, lines 55-58.).

Consider claim 17, Hsin teaches:

providing an optically transmissive substrate(60, figures 2 and 3);

and electrically coupling an integrated circuit(58) including an optical imaging element(The integrated circuit(58) is an optical imaging element, paragraph 013.) with the optically transmissive substrate(The optical imaging element(58) is electrically coupled to said substrate(60) via wires(68) and signal input terminals(64). See figures 2 and 3, paragraph 0013.), and positioning the integrated circuit so that the optical imaging element(58) faces the substrate(60, see figures 2 and 3).

However, Hsin does not explicitly teach associating a filter material, an antireflective material, or both a filter material and an antireflective material with the optically transmissive substrate.

Melman et al. is similar to Hsin in that Melman et al. teach an optical sensor circuit assembly(figures 1-9b), comprising an optically transmissive substrate("cover glass", 806, figures 8a-8c, column 6, line 49), and an optical imaging element("sensor", 116, column 6, line 52, figure 8c) coupled to said substrate(sensor(116) is coupled to filter material(820) with glue layer(800), see figure 8c).

However, in addition to the teachings of Hsin, Melman et al. teach that the optically transmissive substrate includes filter material(cover glass(106) has an antireflective coating(816) and an optical IR blocking coating(820), see figure 8C, column 6, line 57 through column 7, line 6).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to associate filter material and/or antireflective material as taught by Melman et al. with the optically transmissive substrate taught by Hsin for the benefit of preventing excess ghosting and scattered light as is caused by internal reflections of optically transmissive substrates, reducing the number of pieces of the optical sensor circuit assembly, preventing damage to the filter material due to the cleaning of the separate lens module, and correcting color and/or contrast distortion(Melman et al., column 2, lines 1-24, column 6, line 44 through column 7, line 2).

Consider claim 19, and as applied to claim 17 above, Hsin further teaches a lens mount(46) supporting said at least one optical element(84, see figures 2 and 3). However, Hsin does not explicitly teach that the lens mount is coupled to the substrate.

Melman et al. further teach a lens mount("body", 300, see figure 3, the lens is coupled to the substrate via the body(300)) supporting said at least one optical element("lens", 202, figure 3) and coupled to the substrate(See figure 3. Said substrate is labeled "106" in figure 3. Lens mount(300) is coupled to substrate(106) via film leads(302 and 304), column 4, lines 55-58.).

10. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsin in view of Melman et al. as applied to claims 7 and 17 above, and further in view of DiOrio et al.(US Patent Application Publication 2004/0217767).

Consider claim 8, and as applied to claim 7 above, Hsin teaches of a plurality of leads and a plurality of pads(see claim 7 rationale). However, the combination of Hsin and Melman et al. does not explicitly teach that a conductive bump is disposed between said plurality of leads and said plurality of pads.

DiOrio et al. teach of a method for improving the uniformity of the heights of terminals in a device assembled through flip-chip packaging or "chip-on-board" applications(paragraph 0029). Like Hsin, DiOrio et al. are concerned with attaching integrated circuits to circuit boards(see paragraph 0031). DiOrio et al. teach that there is an imminent problem in that if the tops of the terminals do not lie in a plane corresponding to the packaging substrate, a reliable connection cannot be established(see paragraph 0007, figure 2). Therefore, packing is very crucial to the overall functionality of a given device.

In addition to the teachings of Hsin and Melman et al., DiOrio et al. teach that the integrated circuits have conductive bumps("metal bumps", 114, see figure 3, paragraph 0031). After conditioning, these bumps would be connected to conductive pads, and between two circuits as shown in figure 2. DiOrio teaches that these conductive bumps could be solder balls, stacked solder balls, copper pillars, or gold studs(paragraph 0031).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to connect the plurality of leads to the plurality of pads taught by the combination of Hsin and Melman et al. with conductive bumps as taught by DiOrio et al. because conductive bumps eliminate problems of connecting with pins alone such as the pins being flexible and easily becoming misaligned, leading to bad contacts and failed connections, and the problem that the length of pins varies greatly with changing temperature and can lead to a mismatch between the pins(i.e. leads) and the terminals(i.e. pads)(DiOrio et al., paragraph 0004).

Consider claim 18, and as applied to claim 17 above, Hsin further teach:

the step of coupling a circuit member(56) to the substrate(60, see figures 2 and 3); and

wherein the step of coupling an integrated circuit(58) with the optically transmissive substrate(60) includes coupling the optical imaging element(58) to the circuit member(56, see figures 2 and 3, the imaging element and circuit member are coupled using electrically conductive leads(64, 66, 68, paragraph 0013).).

However, the combination of Hsin and Melman et al. does not explicitly teach that the coupling of the optical imaging element to the circuit member is done using conductive bumps.

DiOrio et al. teach of a method for improving the uniformity of the heights of terminals in a device assembled through flip-chip packaging or "chip-on-board" applications(paragraph 0029). Like Hsin, DiOrio et al. are concerned with attaching integrated circuits to circuit boards(see paragraph 0031). DiOrio et al. teach that there is an imminent problem in that if the tops of the terminals do not lie in a plane corresponding to the packaging substrate, a reliable connection cannot be established(see paragraph 0007, figure 2). Therefore, packing is very crucial to the overall functionality of a given device.

In addition to the teachings of Hsin and Melman et al., DiOrio et al. teach that the integrated circuits have conductive bumps("metal bumps", 114, see figure 3, paragraph 0031). After conditioning, these bumps would be connected to conductive pads, and between two circuits as shown in figure 2. DiOrio et al. teach that these conductive bumps could be solder balls, stacked solder balls, copper pillars, or gold studs(paragraph 0031).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to couple the optical imaging element to the circuit member as taught by the combination of Hsin and Melman et al. using conductive bumps as taught by DiOrio et al. because conductive bumps eliminate problems of connecting with pins alone such as the pins being flexible and easily becoming misaligned, leading

to bad contacts and failed connections, and the problem that the length of pins varies greatly with changing temperature and can lead to a mismatch between the pins(i.e. leads) and the terminals(i.e. pads)(DiOrio et al., paragraph 0004).

11. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Melman et al. in view of DiOrio et al.(US Patent Application Publication 2004/0217767).

Consider claim 14, and as applied to claim 11 above, Melman et al. further teach:

said integrated circuit("semiconductor die" 116, column 5, line 46) further comprises a plurality of electrically conductive pads("bonding pads", 512, figure 5b);

and said assembly further comprises: a circuit member("support element", 102, figure 8c) coupled to said substrate(see figure 8c), said circuit member(102) defining a plurality of electrically conductive leads(112, see figure 5b, column 5, lines 54-61).;

However, Melman et al. do not explicitly teach a plurality of conductive bumps disposed between said plurality of leads and said plurality of pads.

DiOrio et al. teach of a method for improving the uniformity of the heights of terminals in a device assembled through flip-chip packaging or "chip-on-board" applications(paragraph 0029). Like Melman et al., DiOrio et al. are concerned with attaching integrated circuits to circuit boards(see paragraph 0031). DiOrio et al. teach that there is an imminent problem in that if the tops of the terminals do not lie in a plane corresponding to the packaging substrate, a reliable connection cannot be

established(see paragraph 0007, figure 2). Therefore, packing is very crucial to the overall functionality of a given device.

In addition to the teachings of Melman et al., DiOrio et al. teach that the integrated circuits have conductive bumps("metal bumps", 114, see figure 3, paragraph 0031). After conditioning, these bumps would be connected to conductive pads, and between two circuits as shown in figure 2. Melman teaches that these conductive bumps could be solder balls, stacked solder balls, copper pillars, or gold studs(paragraph 0031).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time of the invention to connect the plurality of leads to the plurality of pads taught by Melman et al. with conductive bumps as taught by DiOrio et al. because conductive bumps eliminate problems of connecting with pins alone such as the pins being flexible and easily becoming misaligned, leading to bad contacts and failed connections, and the problem that the length of pins varies greatly with changing temperature and can lead to a mismatch between the pins(i.e. leads) and the terminals(i.e. pads)(DiOrio et al., paragraph 0004).

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert H. Cutler whose telephone number is (571)-270-1460. The examiner can normally be reached on Mon-Fri (7:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc-Yen Vu can be reached on (571)-272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

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SUPERVISORY PATENT EXAMINER